AMENDMENTS TO THE CLAIMS:

The following listing of claims supersedes all prior versions and listings of claims in this application:

1. (Currently Amended) A memory configuration for use in a computer system, the memory comprising:

a plurality of address decoders, each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states; and

a data memory having a plurality of word lines of predetermined length,

each of the said address decoders being activatable to select one of the plurality of word lines;

the address decoders including means to receive an input address having a predetermined number of bits and means to compare the identifier of an address decoder with the input address; and

wherein the memory further includes means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier; and

wherein each address decoder identifier has an equal number of bits set to the first selectable state and the means to receive an input address [[in]] is configured to receive addresses containing a predetermined number of bits set to the first selectable state.

2. (Currently Amended) A memory configuration according to claim 1, wherein:

the means to compare the identifier of an address decoder with the input address considers positional correspondence between bits set to the first selectable [[sate]] state in the input address and bits set to the first selectable state in the decoder identifiers.

3-4. Cancelled.

5. (Previously Presented) A memory configuration according to claim 1, wherein the predetermined number of bits set to the first selectable state in an input address is equal to the number of bits set to the first selectable state in each of the address decoder identifiers.

6. (Previously Presented) A memory configuration according to claim 1, wherein the data memory comprises a plurality of single bit memories, such that each bit of each word line is stored in a single bit memory.

7. (Previously Presented) A memory configuration according to claim 1, wherein the data memory comprises a data input line containing an equal number of bits to each of the plurality of word lines.

8. (Original) A memory configuration according to claim 7, further comprising data writing means to copy data from the data input line to word lines activated by the address decoders.

9. (Previously Presented) A memory configuration according to claim 7, wherein the data input line is configured to receive input data containing a predetermined number of bits set to the first selectable state.

10. (Previously Presented) A memory configuration according to claim 1, further comprising:

means to sum values stored at each bit of word lines activated by an address decoder to generate an activation level value for each bit.

11. (Previously Presented) A memory configuration according to claim 9, further comprising:

means to generate an output word containing the predetermined number of bits set to the first selectable state.

12. (Original) A memory configuration according to claim 11, wherein the bits set to first selectable state in the output are the predetermined number of bits having the highest activation level.

13. (Currently Amended) A memory configuration according to claim 1, wherein the memory is implemented using a plurality of artificial neurons connected together to form a neural network.

14. (Original) A memory configuration according to claim 13, wherein the plurality of address decoders are represented by a plurality of address decoder neurons, and the data memory is represented by a plurality of data neurons.

15. (Previously Presented) A neural network memory configuration for use in a computer system, the memory comprising:

a plurality of address decoder neurons each of which is connected to a predetermined number of input neurons;

a data memory having a plurality data neurons, each of the said address decoder neurons being activatable to select some of the plurality of data neurons;

the address decoder neurons including means to receive a signal representing a firing of an input neuron to which it is connected; and

wherein an address decoder neuron comprises means to activate data neurons if firing signals are received from at least a predetermined minimum number of input neurons to which the address decoder neuron is connected.

16. (Previously Presented) A method for operating a memory for use in a computer system, the memory comprising:

a plurality of address decoders each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states;

a data memory having a plurality of word lines of predetermined length, each of the said address decoders being activatable to select one of the plurality of word lines;

wherein an input address having a predetermined number of bits is input to the address decoder, the identifier of an address decoder is compared with the input address and address decoders are activated if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier;

wherein each address decoder identifier has an equal number of bits set to the first selectable state; and

wherein an input address has a predetermined number of bits set to the first selectable state.

17. (Original) A method according to claim 16, wherein input data is presented at a data input of the data memory and the data is written to word lines activated by the activated address decoders.

18. (Previously Presented) A method according to claim 16, wherein the predetermined minimum number of bits is set such that fewer than 100 address decoders are activated by any valid input address.

19. (Previously Presented) A method according to claim 18, wherein the predetermined minimum number of bits is set such that fewer than 50 address decoders are activated by any valid input address.

20. (Original) A method according to claim 19, wherein the predetermined minimum number of bits is set such that fewer than 20 and more than 11 address decoders are activated by any valid input address.

21. (Previously Presented) A method for optimizing the operation of a computer memory which comprises a plurality of address decoders each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states, a data memory having a plurality of word lines of predetermined length, each of the said address decoders being activatable to select one of the plurality of word lines, means to receive an input address, and means to activate one or more of the

address decoders if a comparison between a decoder identifier and the input address exceeds a predetermined comparison threshold; said method comprising:

determining an operationally beneficial number of address decoders to be activated in response to a valid input address, and

configuring the comparison threshold such that a valid input address will activate a number of address decoders equal to the operationally beneficial number of address decoders to be activated.

22. (Original) A method according to claim 21, wherein the comparison compares the number of bits set to the first selectable state in the input address with the number of bits set to the first selectable state in each of the address decoder identifiers.

23. (Previously Presented) A method according to claim 21, wherein the operationally beneficial number is determined so as to allow maximum error free data recovery from the data memory.

24. (Currently Amended) A method according to, claim 23, wherein the operationally beneficial number is determined using a function of the form:

$$w=f(h, P_c, D, d)$$

where:

w is the operationally beneficial number of address decoders to be activated;

h is the probability of an arbitrary bit in the data memory being set to the first selectable state;

D is the number of bits in each word line, and each word line has d bits set to the first selectable state; and

P_c is the probability of a bit being correctly recovered from the data store[[;]].

25. (Original) A method according to claim 24, wherein the function is:

$$h^{-w} \cdot w = \frac{\ln(1-h)}{\ln(P_c)} \cdot W \cdot \frac{D}{d} \cdot (D-d)$$

26. (Previously Presented) A method according to claim 21, wherein the operationally beneficial number of address decoders to be activated is determined so as to allow maximum error free data recovery, while allowing some data to be recovered with errors.

27. (Original) A method according to claim 26, wherein the operationally beneficial number is determined using a function of the form:

$$w=f(h, D, d)$$

where:

w is the operationally beneficial number of address decoders to be activated;

h is the probability of an arbitrary bit in the data memory being set to the first selectable state;

D is the number of bits in each word line, and each word line has d bits set to the first selectable state.

28. (Original) A method according to claim 27, wherein the function is:

$$\frac{(h^{-w}-1)}{w} = -(D-d)\cdot \ln h$$

29. (Previously Presented) A method according to claim 21, wherein the operationally beneficial number w is set so as to have a value no less than that given by the equation:

$$\frac{(h^{-w}-1)}{w} = -(D-d)\cdot \ln h$$

and no more than that given by the equation:

$$h^{-w} \cdot w = \frac{\ln(1-h)}{\ln(P_c)} \cdot W \cdot \frac{D}{d} \cdot (D-d)$$

30. Cancelled.

31. (Previously Presented) A computer-readable storage medium containing a computer program which, when executed by a computer, carries out the method of claim 16.

32-34. Cancelled.

35. (Previously Presented) A memory configuration for use in a computer system, the memory comprising:

a plurality of address decoders each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states;

a data memory having a plurality of word lines of predetermined length, each of the said address decoders being activatable to select a predetermined one of the plurality of word lines;

the address decoders comprising means to receive an input address having a predetermined number of bits and means to compare the identifier of an address decoder with the input address, and

wherein the memory further comprises means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier.

36. (Previously Presented) A method for operating a memory for use in a computer system, the method comprising:

allocating to each of a plurality of address decoders an identifier having a predetermined number of bits, each bit having first and second selectable states; and

activating each of said address decoders to select a predetermined one of a plurality of word lines in a data memory having a plurality of word lines of predetermined length,

wherein an input address having a predetermined number of bits is input to the address decoder, the identifier of an address decoder is compared with the input address and address decoders are activated if at least a predetermined minimum number of bits

set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier.

37. (Previously Presented) A memory configuration for use in a computer system, the memory comprising:

a plurality of address decoders, each of which is allocated an identifier having a predetermined number of bits, each bit having first and second selectable states; and

a data memory having a plurality of word lines of predetermined length, each of the said address decoders being activatable to select one of the plurality of word lines;

the address decoders including means to receive an input address having a predetermined number of bits and means to compare the identifier of an address decoder with the input address;

wherein the memory further includes means to activate an address decoder if at least a predetermined minimum number of bits set to the first selectable state in the input address correspond to bits set to the first selectable state in the decoder identifier;

wherein the data memory comprises a plurality of single bit memories, such that each bit of each word line is stored in a single bit memory; and

wherein the data memory comprises a data input line containing an equal number of bits to each of the plurality of word lines, the data input line being configured to receive input data containing a predetermined number of bits set to the first selectable state.